

Figure 1(a). Gate to common short defects in TFT array with double common line layout.

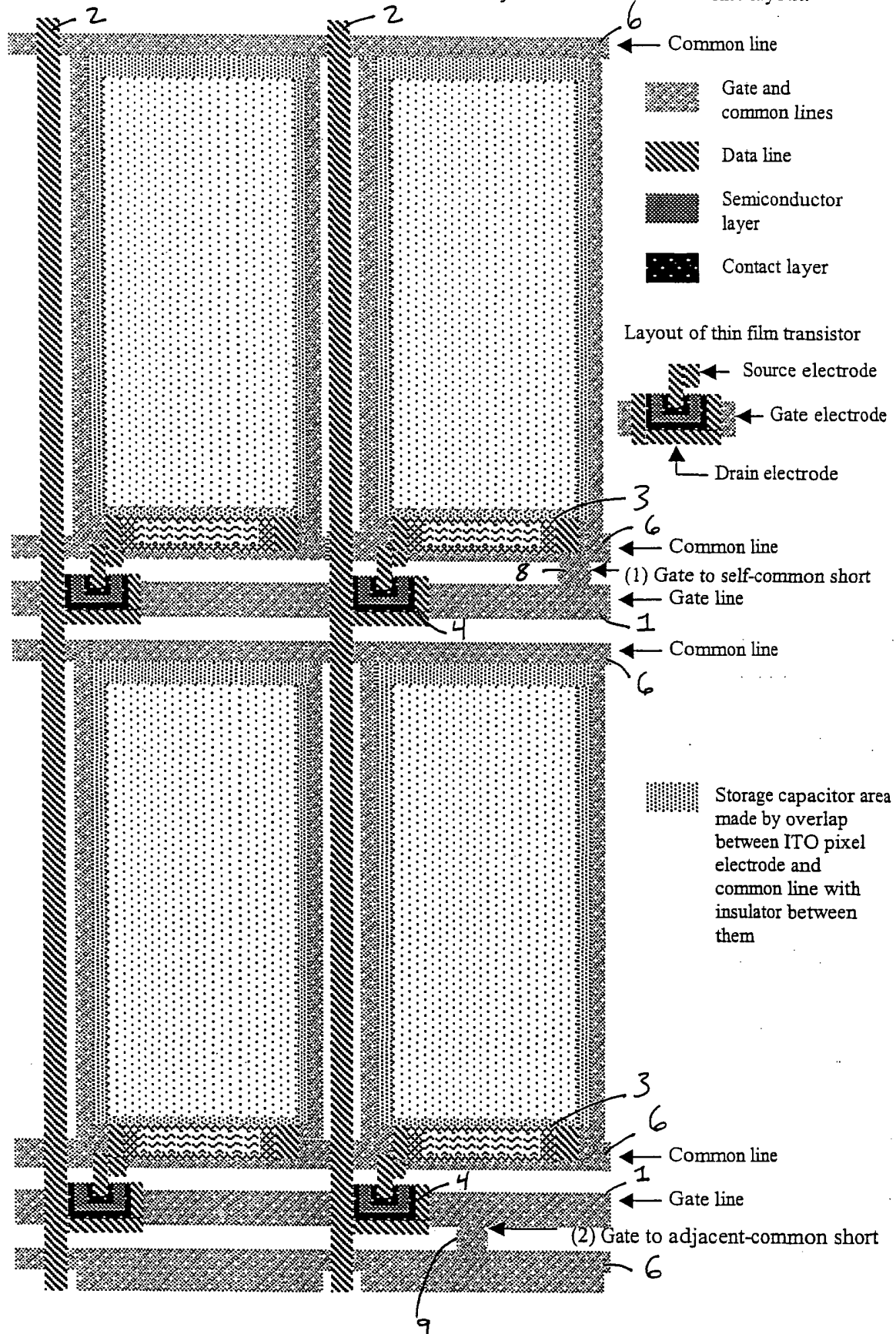


Figure 1(b). Explanation of pixel layout by showing four pixels in different process step.

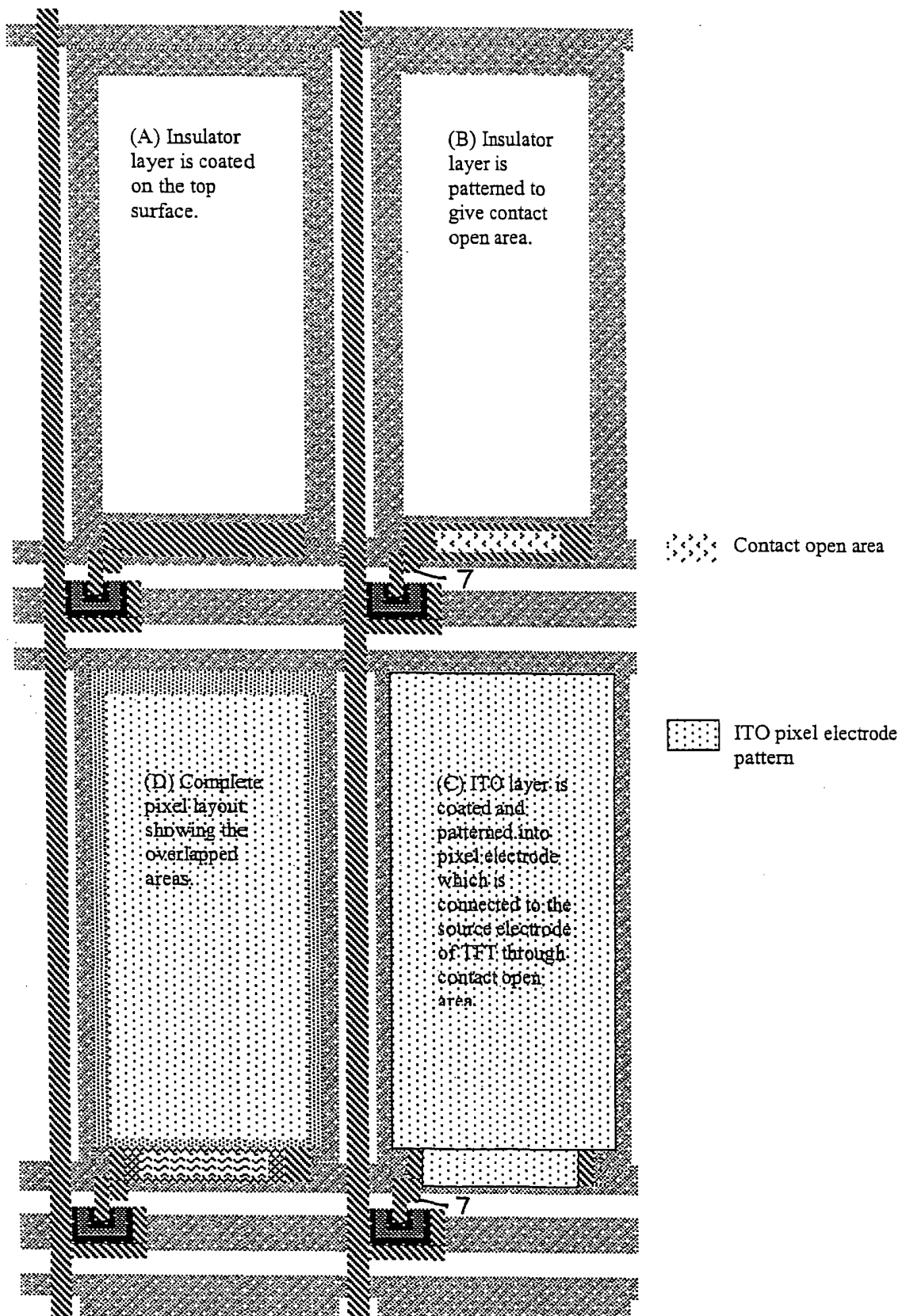
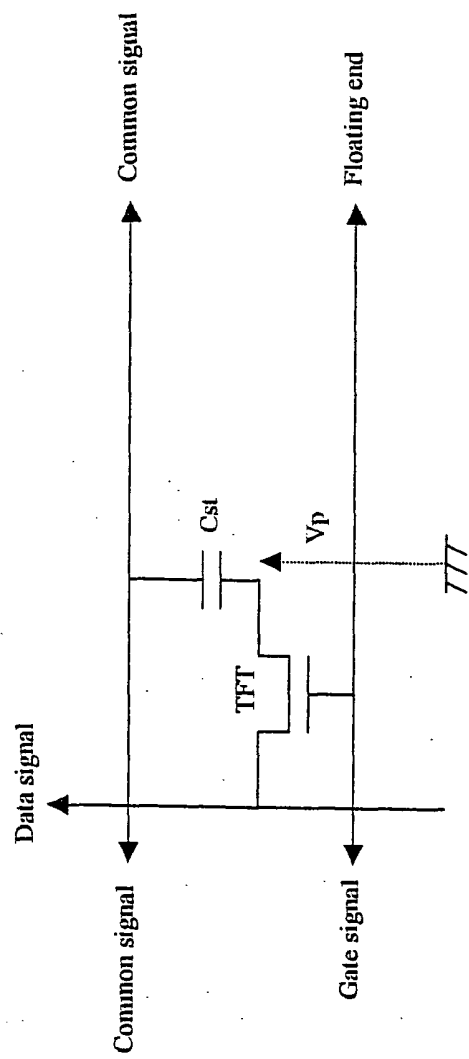


Figure 3. Simplified equivalent circuit of one cross point in TFT array.



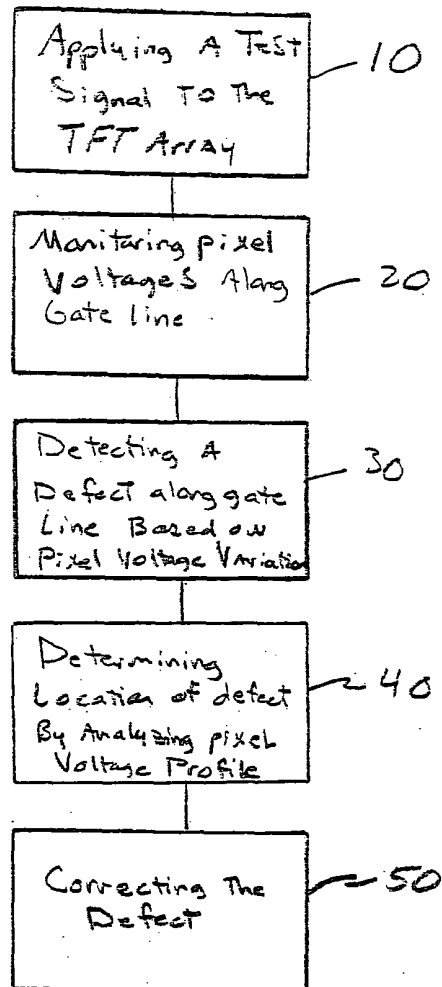


Fig. 3

Signal patterns to detect the short defect between gate and common lines.

Fig. 4(a) Signal patterns for positive pixel voltage

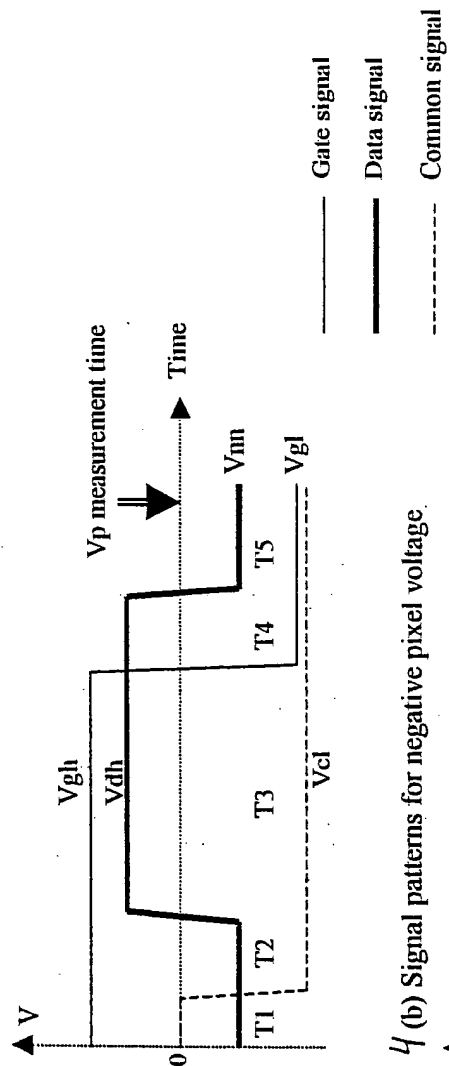
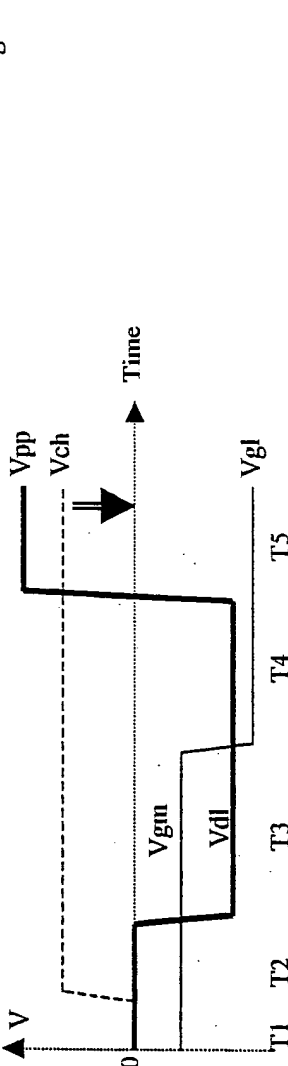


Fig. 4(b) Signal patterns for negative pixel voltage



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Figure 4 Analysis of pixel voltages along the gate line with a short defect between gate and self-common lines when the signal patterns of Fig. 2 (a) is applied.

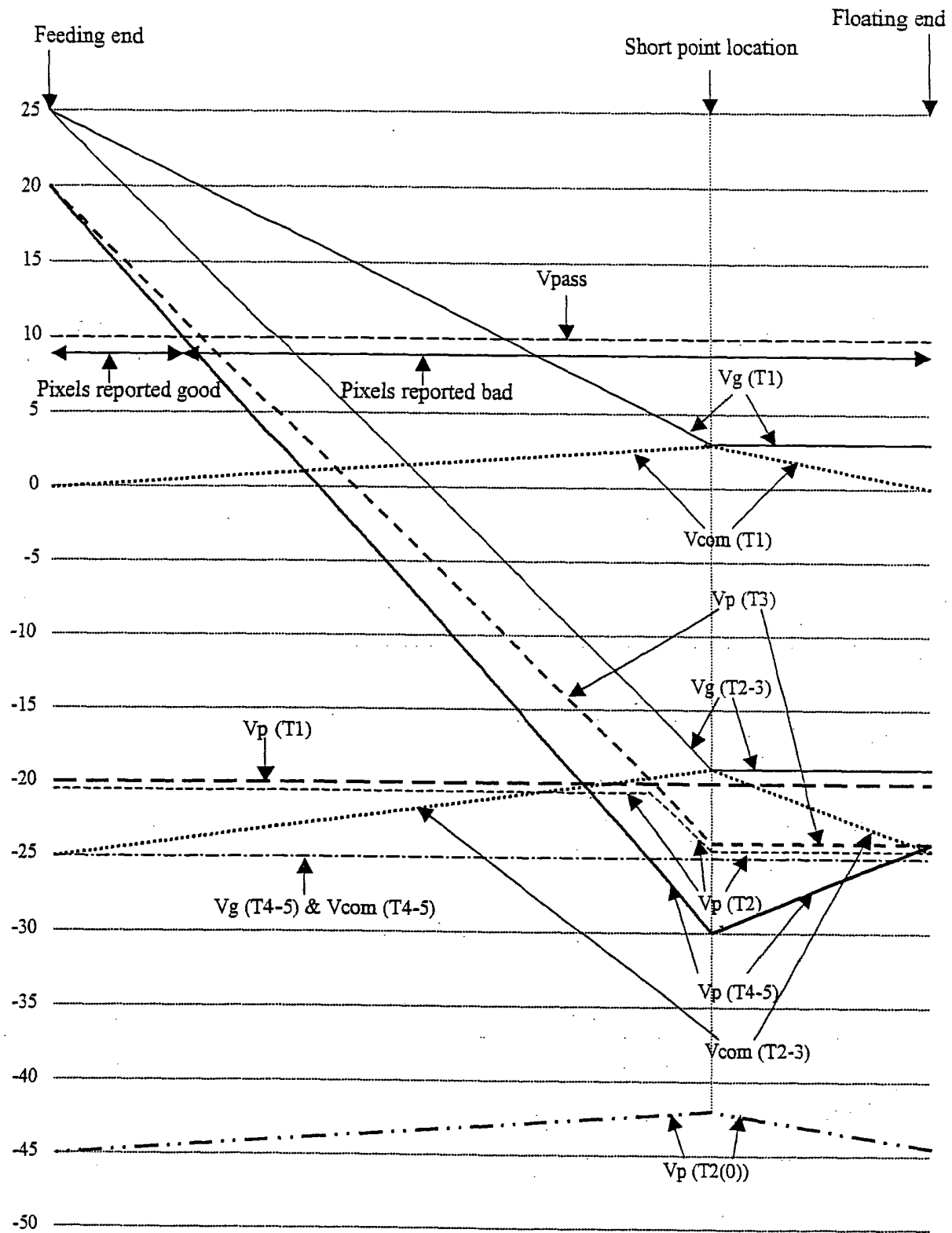
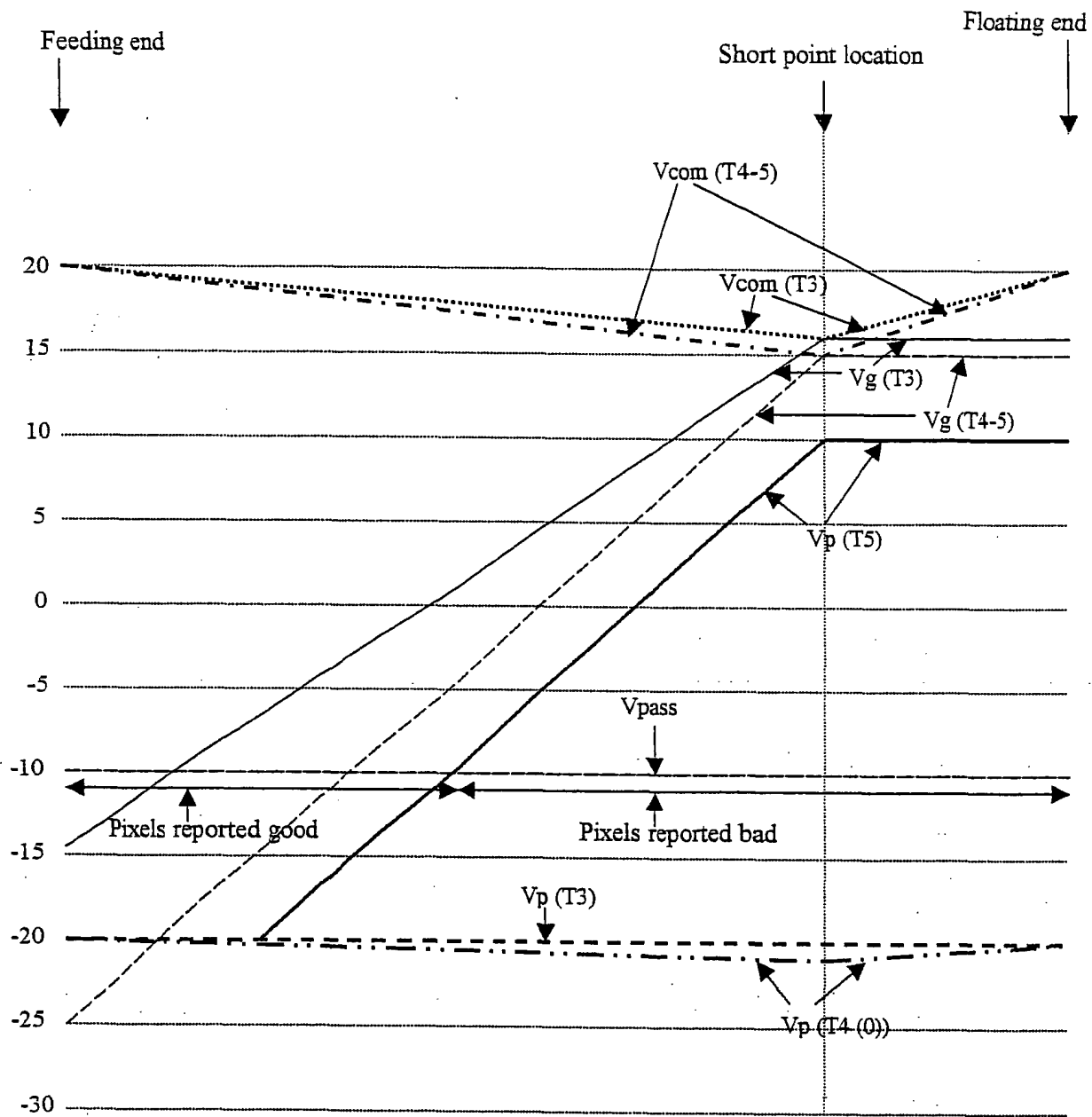


Figure 5. Analysis of pixel voltages along the gate line with a short defect between gate and self-common lines when the signal patterns of Fig. 2 (b) is applied.



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Figure 7 Calculation of pixel voltages (V_p (T4-5) of Fig 4 - V_p (T5) of Fig 5) along the gate line with a short defect between gate and self-common lines.

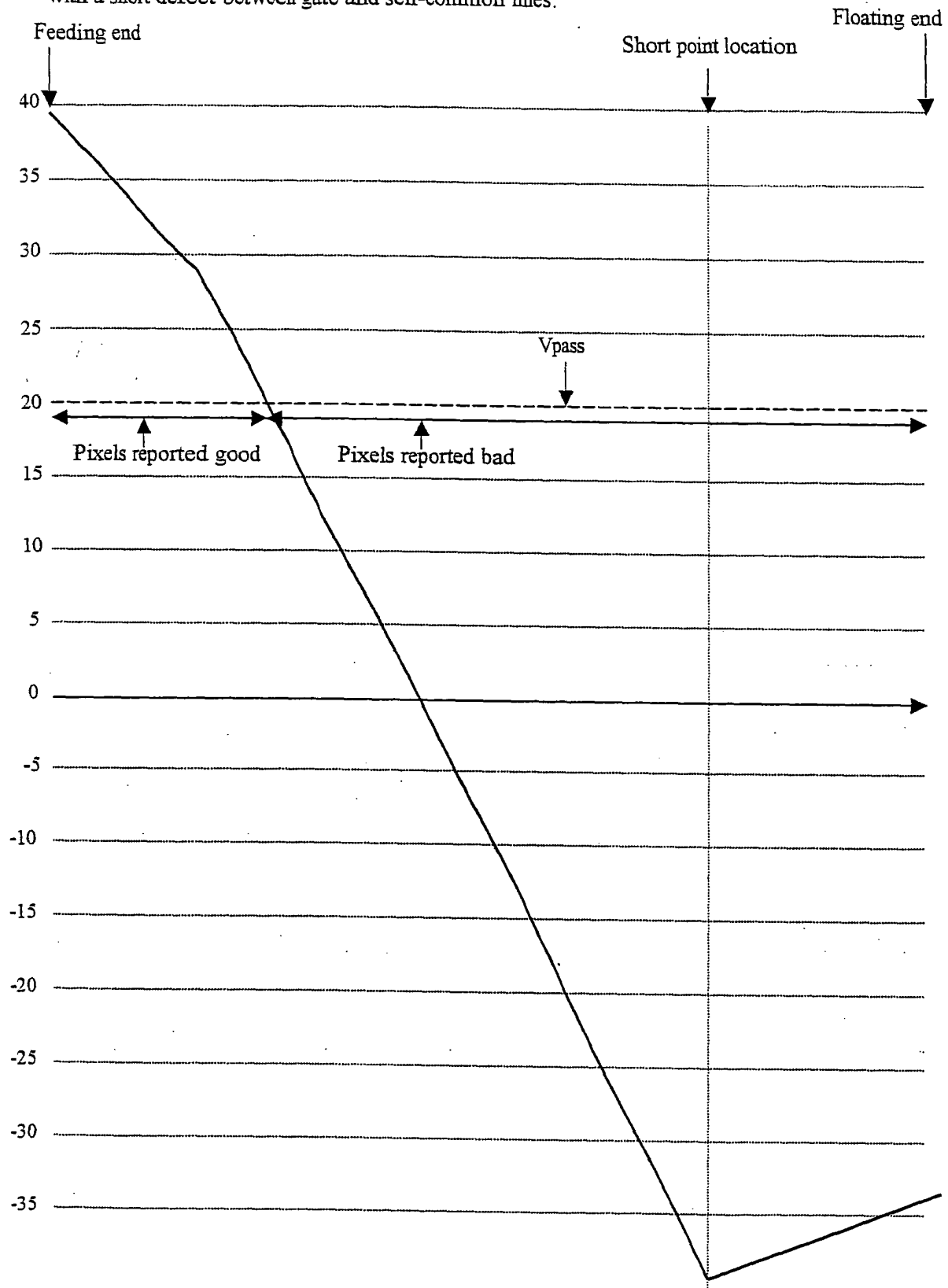


Figure 7. Analysis of pixel voltages along the gate line with a short defect between gate and adjacent-common lines when the signal patterns of Fig. 2 (a) is applied.

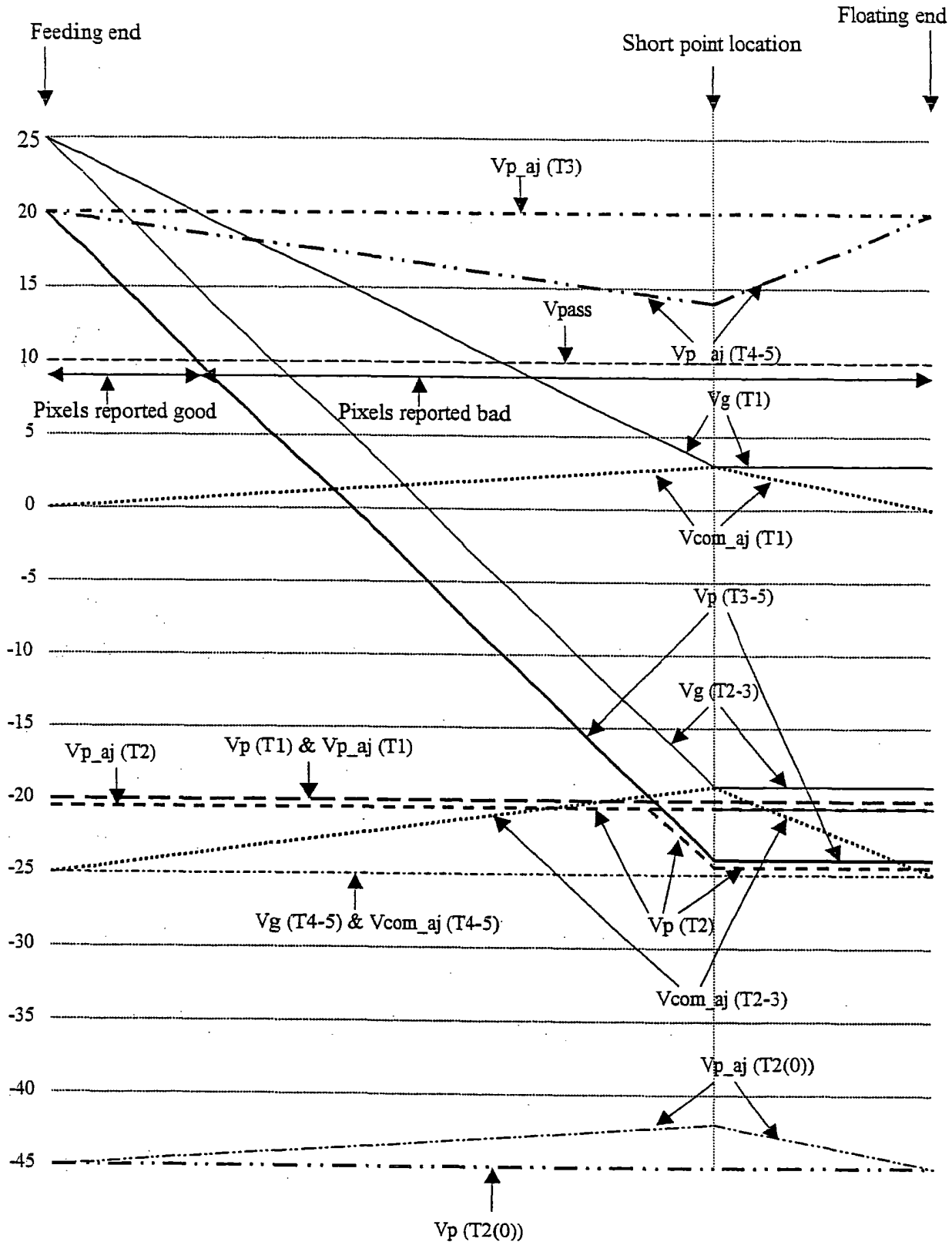
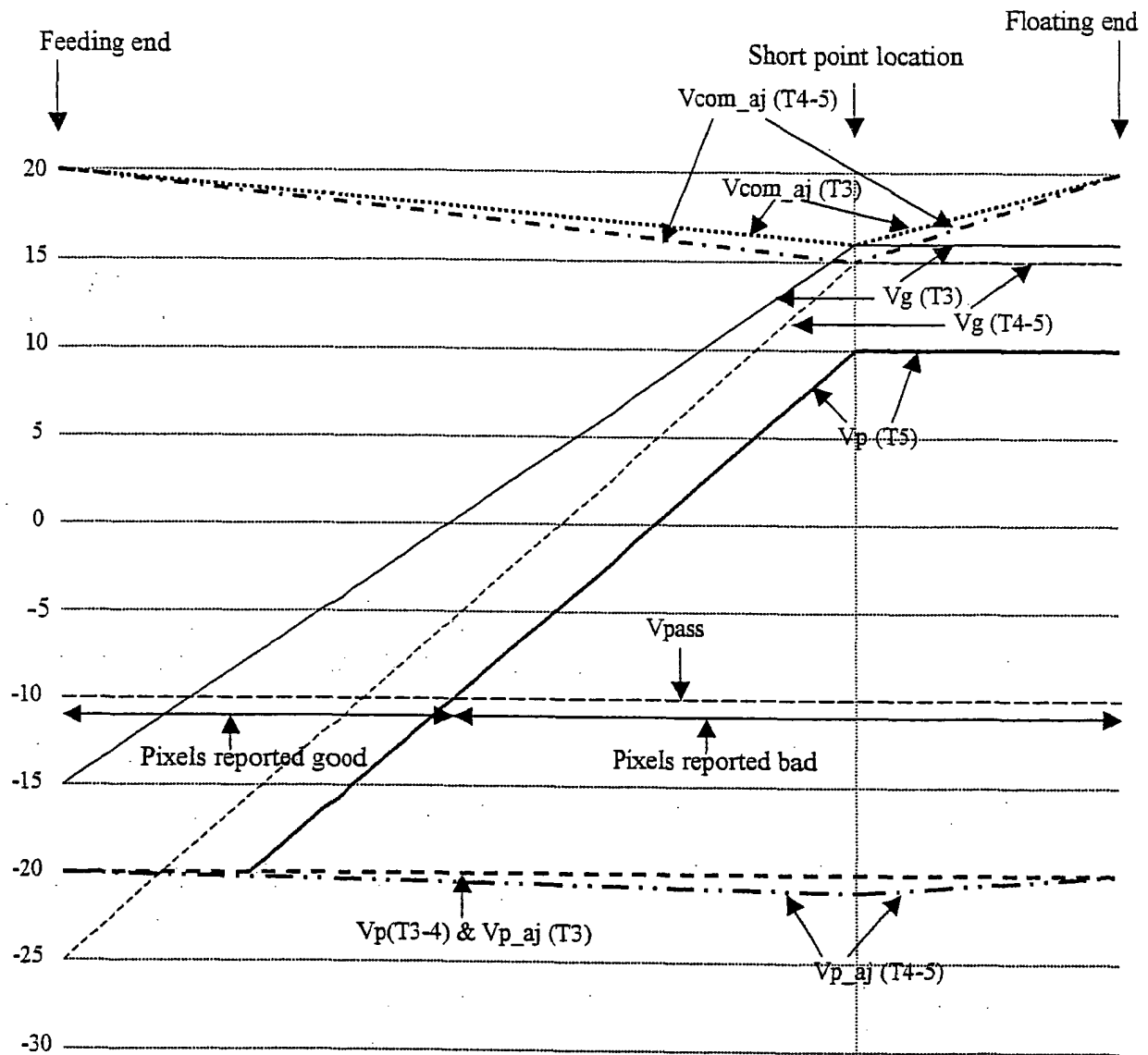
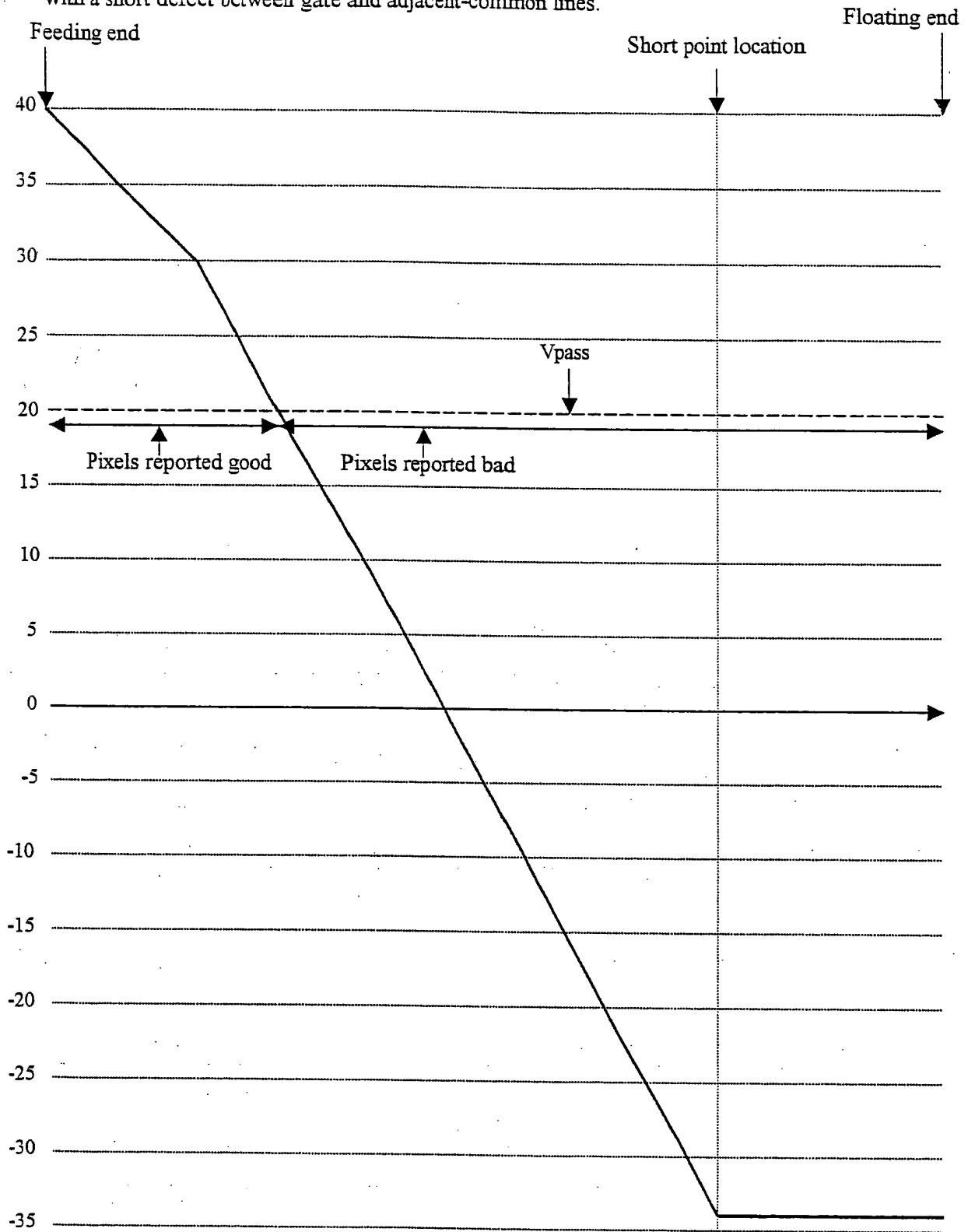


Figure 8. Analysis of pixel voltages along the gate line with a short defect between gate and adjacent-common lines when the signal patterns of Fig. 2 (b) is applied.



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Figure 9. Calculation of pixel voltages (V_p (T3-5) of Fig 7 – V_p (T5) of Fig 8) along the gate line with a short defect between gate and adjacent-common lines.



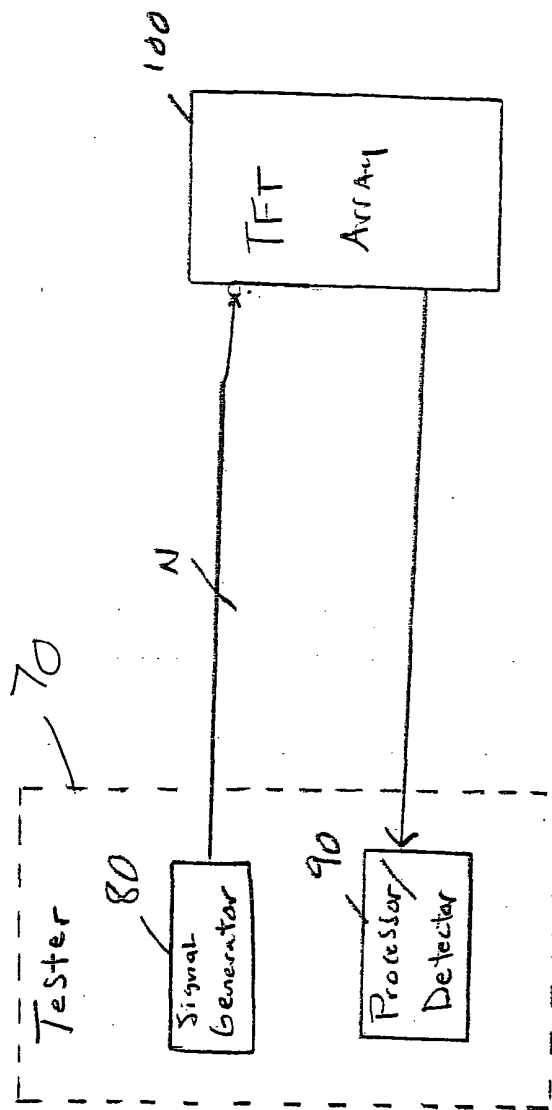


Fig. 11

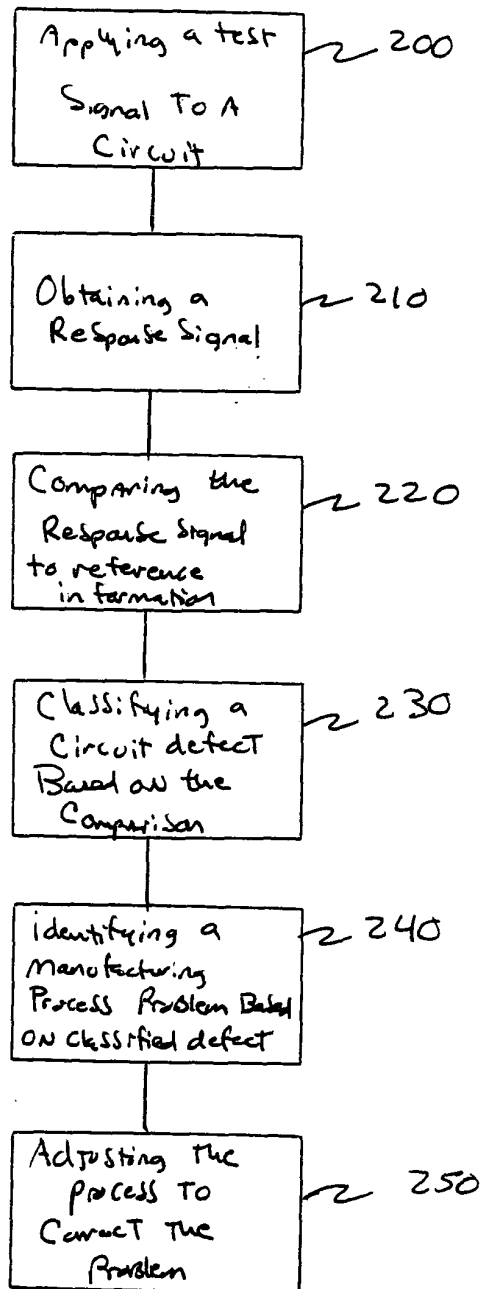
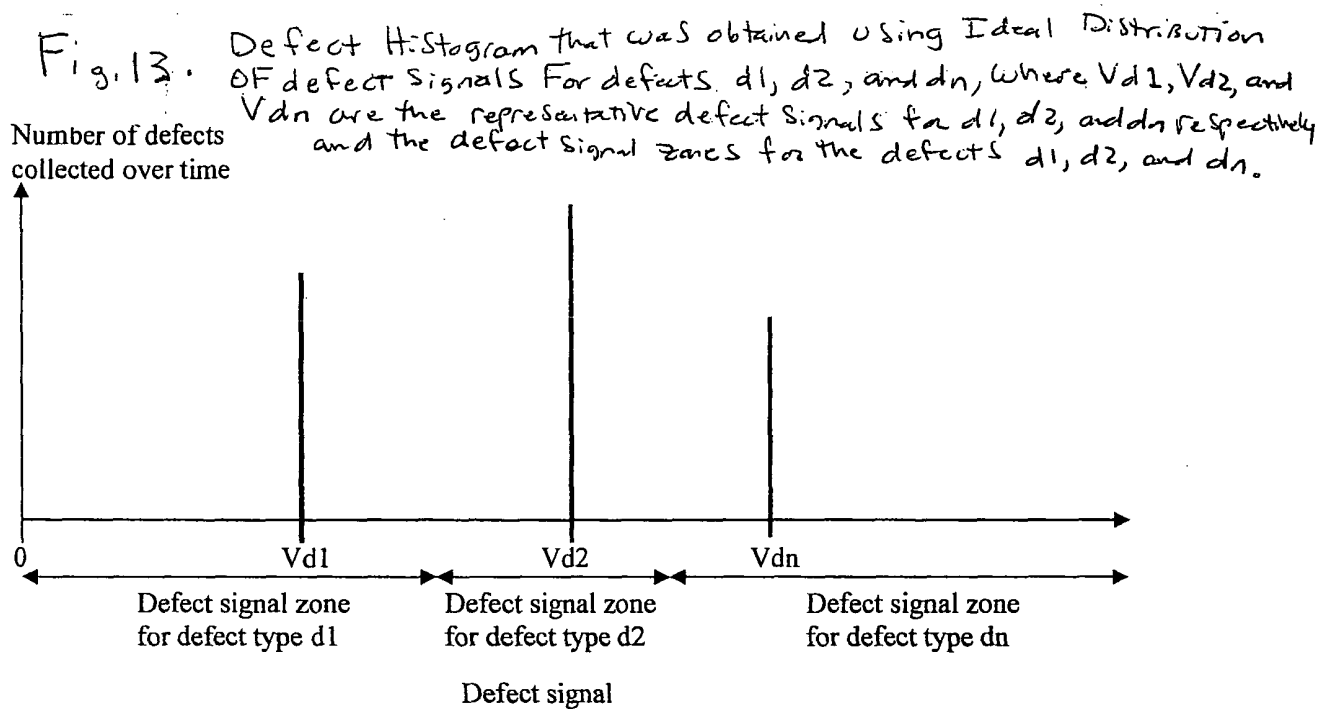
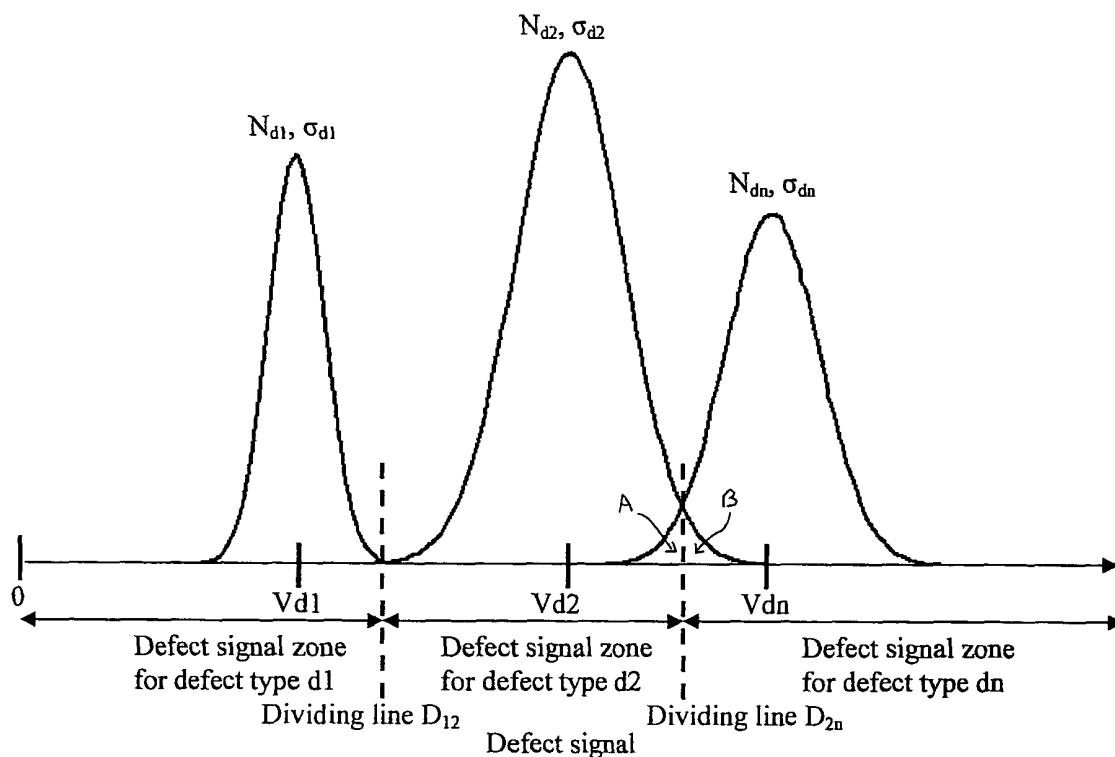


Figure 12

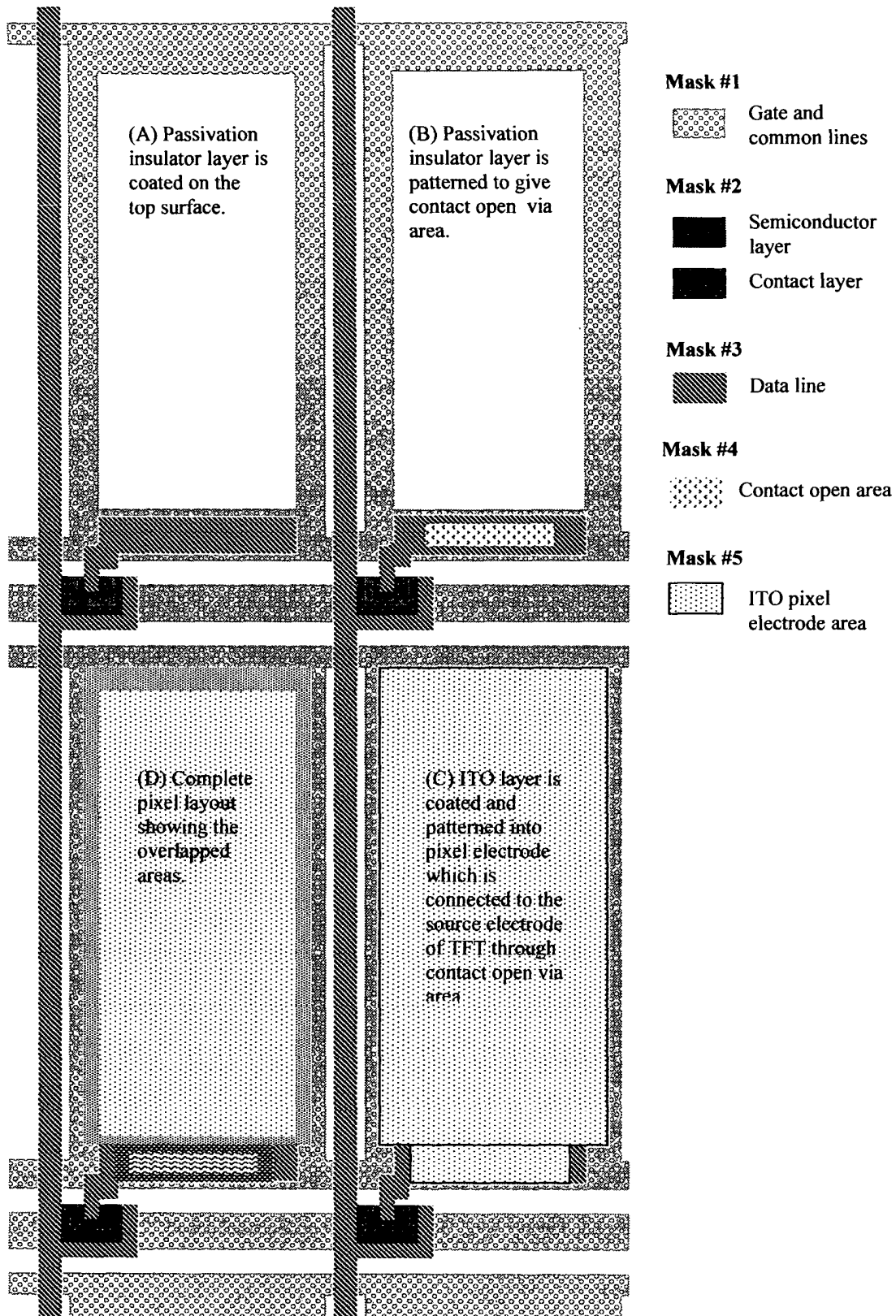


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Figure 2. Realistic distribution of the defect signals for the defects d_1, d_2 , and d_n , where normal distribution function is used for each defect type.



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Figure 3(b). Explanation of pixel layout by showing four pixels in different process step.



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Figure 4. Example of the process flow for TFT-array in Fig. 3.

